WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit on a semiconductor chip, comprising:

a plurality of terminals connected to outside;

buffers and protection circuits connected to the terminals;

a plurality of regulators which step down a first power voltage which is supplied from the outside to a certain terminal thereby to produce at least one kind of internal power voltage which is lower than the first power voltage; and

a first internal circuit which operates based on the internal power voltage,

wherein the regulators are set in an area including the buffers and protection circuits, and its width is generally determinable from the layout width of the buffers and protection circuits.

2. A semiconductor integrated circuit according to claim 1, further comprising:

a power line connected to the outputs of the regulators and providing the internal power voltage to the first internal circuit.

3. A semiconductor integrated circuit according to claim 2, wherein the power line is formed in a closed loop.

4. A semiconductor integrated circuit according to claim 3, wherein the power line contains a generally equal parasitic

resistance of line segments between output nodes of the voltage regulators.

5. A semiconductor integrated circuit according to claim 3, wherein the power line includes a generally equal length of line segments between output nodes of the voltage regulators.

6. A semiconductor integrated circuit according to claim 2, further comprising:

a terminal connected to said power line.

7. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit operatable based on the first power voltage,

wherein the second internal circuit includes a converting circuit which converts the signal outputted from the first internal circuit to logic levels derived from the first power voltage.

8. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit operatable based on the first power voltage,

wherein the second internal circuit includes a reference voltage generation circuit providing a reference voltage for a step-down voltage to the regulators.

9. A semiconductor integrated circuit according to claim 8, further comprising:

a reference voltage line formed in an open loop for providing the reference voltage to the regulators.

10. A semiconductor integrated circuit according to claim 9, wherein the reference voltage line is laid to run generally along the layout of the regulators, with a shield line having the ground voltage being formed in parallel thereto on the same wiring layer.

11. A semiconductor integrated circuit according to claim 10, further comprising: shield lines or shield areas formed above and below the reference voltage line.

12. A semiconductor integrated circuit according to claim 8, wherein the reference voltage generation circuit provides the reference voltage based on the output voltage of a reference voltage generator having its circuit characteristics determined by trimming information, and includes an electrically-writable nonvolatile memory storable the trimming information.

13. A semiconductor integrated circuit according to claim 8, wherein the reference voltage generation circuit is capable of outputting a reference voltage based on selection from among a plurality of reference voltages.

14. A semiconductor integrated circuit according to claim 13, wherein the reference voltage generation circuit is capable of selecting a reference voltage in response to a signal provided from a control unit depending on the operation mode.

15. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit which operates based the first power voltage,

wherein the second internal circuit comprising an activation control unit which turns on or off the regulators.

16. A semiconductor integrated circuit according to claim 15, wherein the activation control unit is capable of turning on or off each of or each group of regulators separately.

17. A semiconductor integrated circuit according to claim 15, wherein one or multiple ones of the voltage regulators have a smaller current supply capacity or smaller power consumption relative to the rest,

wherein the activation control unit turns on all of the regulators or regulators excluding the regulator(s) having a smaller current supply capacity or smaller power consumption in response to a first operation mode of the integrated circuit, and turns on the voltage regulator(s) having a smaller current supply capacity or smaller power consumption in response to a second operation mode of the integrated circuit.

18. A semiconductor integrated circuit according to claim 15, wherein the second internal circuit includes a sub regulator which is smaller in current supply capacity or power consumption than the regulators, the activation control means turning on the regulators in response to a first operation mode of the integrated circuit, and turning on the sub regulator in response to a second operation mode of the integrated circuit.

19. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit operatable based on the first power voltage;

a power line connected to the outputs of the regulators and providing the internal power voltage to the first internal circuit; and

a terminal connected to the power line,

wherein the second internal circuit includes a driver control circuit for a switching regulator, the integrated circuit further includes a terminal which is assigned to the external output terminal of the drive control signal produced by the driver control circuit.

20. A semiconductor integrated circuit according to claim 19, further comprising:

a deactivation control unit which deactivates one of the regulators or the driver control circuit permanently.

21. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit which operates based on the first power voltage,

wherein the second internal circuit includes a substrate bias control circuit which controls the substrate voltage of switching elements included in the first internal circuit, and

wherein the substrate bias control circuit operates based

on the first power voltage and the internal power voltage to control the substrate voltage depending on the operation mode of the integrated circuit.

22. A semiconductor integrated circuit according to claim 1, further comprising:

a second internal circuit which operates based on the first power voltage,

wherein the second internal circuit includes a substrate bias control circuit which controls the substrate voltage of switching elements included in the first internal circuit, and

wherein said substrate bias control circuit operates based on the first power voltage and the internal power voltage to apply a negative bias for substrate to the switching elements in the standby mode of the first internal circuit.

23. A semiconductor integrated circuit according to claim 21, wherein the substrate bias control circuit provides the substrate voltages in the first internal circuit, which are derived from the internal power voltage and a ground voltage in response to a first operation mode of the integrated circuit, and provides the substrate voltages in the first internal circuit, which are derived from the first power voltage and a negative voltage which is produced by stepping down a ground voltage in response to a second operation mode of the integrated circuit.

24. A method of designing a semiconductor integrated circuit comprising:

a plurality of terminals connected to outside;

a plurality of buffers and protection circuits connected to said terminal;

a plurality of regulators which step down a first power voltage which is supplied from the outside to a certain terminal thereby to produce at least one kind of internal power voltage which is lower than the first power voltage; and

a first internal circuit operatable based on the internal power voltage,

wherein the method including a step of laying said regulators in an area having its width generally determined from the layout width of said buffers and at positions near the external terminals for receiving the first power voltage and a ground voltage.

25. A method of designing a semiconductor integrated circuit according to claim 24,

wherein the step of said method includes steps of setting regulators which are selected from a cell library depending on the current capacity needed by said first internal circuit.

26. A semiconductor integrated circuit on a semiconductor chip comprising:

a first area which lays a plurality of terminals connected to outside;

a second area which lays buffers and protection circuits connected to said terminals, and a plurality of voltage

regulators which step down a first power voltage which is supplied from the outside to a certain terminal thereby to produce at least one kind of internal power voltage which is lower than the first power voltage;

a third area which lays a first internal circuit which operates based on the internal power voltage; and

a fourth area which lays a second internal circuit which operates based on the first power voltage,

wherein said regulators are laid at positions near the terminals for receiving the first power voltage and a ground voltage, and connected to a power line, and

wherein said power line provides the internal power voltage to said first internal circuit.

27. A semiconductor integrated circuit according to claim 26, wherein said power line is formed to be a closed loop and include a generally equal parasitic resistance of line segments between output nodes of said voltage regulators.

28. A semiconductor integrated circuit according to claim 27 further comprising a terminal connected to said power line.

29. A semiconductor integrated circuit on a semiconductor chip, comprising:

a plurality of terminals connected to outside;

buffers and protection circuits connected to said terminals;

a plurality of regulators which step down a first power

voltage which is supplied from the outside to a certain terminal thereby to produce at least one kind of internal power voltage which is lower than the first power voltage;

a first internal circuit operatable based on the internal power voltage; and

a second internal circuit operatable based on the first power voltage,

wherein said regulators is laid near the terminals for receiving the first power voltage and a ground voltage, and connected to a power line,

wherein said power line provides the internal power voltage to said first internal circuit,

wherein said second internal circuit includes a signal level converting circuit which converts the signal outputted from said first internal circuit to have logic levels derived from the first power voltage, a reference voltage generation circuit which provides a reference voltage for a step-down voltage to said regulators, and a CPU, and

wherein said reference voltage generation circuit is capable of outputting a reference voltage based on selection from among a plurality of reference voltages and adapted to select a reference voltage in response to a signal which is given by said CPU.

30. A semiconductor integrated circuit on a semiconductor chip comprising:

a plurality of terminals connected to outside;

buffers and protection circuits connected to said terminals;

a plurality of regulators; and

a first internal circuit,

wherein said regulators step down a first power voltage supplied from the outside thereby to produce at least one kind of internal power voltage which is lower than the first power voltage,

wherein said first internal circuit operates based on the internal power voltage, and

wherein said regulators each includes a transistor circuit formed of an amplifier circuit and at least one transistor.

31. A semiconductor integrated circuit according to claim 30, wherein said amplifier circuit is located within the area where said terminals, buffers and protection circuits are arranged, and said transistor circuit is located inner than said terminals, buffers and protection circuits on said semiconductor chip.

32. A semiconductor integrated circuit according to claim 30,

wherein said area of terminals, buffers and protection circuits extends along at least one side of said semiconductor chip,

wherein said amplifier circuit is within said area of terminals, buffers and protection circuits, and

wherein said transistor circuit is inner than said area

of amplifier circuit on said semiconductor chip.

33. A semiconductor integrated circuit on a semiconductor chip comprising:

a terminal area including a plurality of terminals connected to outside;

a first circuit area where buffers and protection circuits connected to said terminals are formed, said first circuit area including a plurality of regulators which step down a first power voltage supplied from the outside thereby to produce at least one kind of internal power voltage which is lower than the first power voltage;

a second circuit area where a first internal circuit operating based on the internal power voltage is laid; and

a third circuit area where a second internal circuit operating based on the first power voltage is laid,

wherein said regulators each includes a transistor circuit formed of an amplifier circuit and at least one transistor, and

wherein said amplifier circuit is located within said first circuit area.

34. A semiconductor integrated circuit according to claim 33, wherein said transistor circuit is located between said first circuit area and said second circuit area, or between said first circuit area and said third circuit area.

35. A semiconductor integrated circuit according to claim 33, wherein said transistor circuit is located inner than said first

circuit area and outer than said second circuit area and third circuit area on said semiconductor chip.